

# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/709,798	05/28/2004	Paul D. Kartschoke	BUR920040003US1	3797		
23389	7590 04/05/2006		EXAMINER			
*	COTT MURPHY & PR N CITY PLAZA	PARIHAR, SUCHIN				
SUITE 300	N CITT PLAZA	•,	ART UNIT	PAPER NUMBER		
GARDEN CITY, NY 11530			2825			
			DATE MAILED: 04/05/200	6		

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application	No.	Applicant(s)		(A)		
Office Action Summary		10/709,798		KARTSCHOKE ET AL.				
		Examiner		Art Unit				
		Suchin Paril	nar	2825				
Period fo	The MAILING DATE of this communication app or Reply	pears on the d	over sheet with the c	orrespondence a	ddress			
WHIC - Exter after - If NO - Failui Any r	CRIENED STATUTORY PERIOD FOR REPL' CHEVER IS LONGER, FROM THE MAILING DATE is ions of time may be available under the provisions of 37 CFR 1.1 SIX (6) MONTHS from the mailing date of this communication. Period for reply is specified above, the maximum statutory period ver to reply within the set or extended period for reply will, by statute eply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS 36(a). In no event will apply and will e c, cause the applica	S COMMUNICATION, however, may a reply be time expire SIX (6) MONTHS from the store to become ABANDONEI	I. lely filed the mailing date of this of (35 U.S.C. § 133).				
Status								
1)🖂	Responsive to communication(s) filed on 28 M	lay 2004.						
2a)□	This action is <b>FINAL</b> . 2b) ☐ This	action is no	n-final.					
3)🖂	)⊠ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
	closed in accordance with the practice under E	Ex parte Qua	/le, 1935 C.D. 11, 45	3 O.G. 213.				
Dispositi	on of Claims							
4)🖂	Claim(s) 1-20 is/are pending in the application.							
	4a) Of the above claim(s) is/are withdraw	wn from cons	ideration.					
5)	Claim(s) is/are allowed.							
6)	Claim(s) is/are rejected.							
7)🖾	Claim(s) <u>1-20</u> is/are objected to.							
8)□	Claim(s) are subject to restriction and/or	r election rec	uirement.					
Application	on Papers							
9)🔲 -	The specification is objected to by the Examine	er.						
10)🛛	The drawing(s) filed on <u>28 May 2004</u> is/are: a)	□ accepted	or b)□ objected to b	y the Examiner.				
	Applicant may not request that any objection to the	drawing(s) be	held in abeyance. See	37 CFR 1.85(a).				
	Replacement drawing sheet(s) including the correct	tion is required	if the drawing(s) is obj	ected to. See 37 C	FR 1.121(d)	١.		
11) 🔲 -	The oath or declaration is objected to by the Ex	caminer. Note	the attached Office	Action or form P	TO-152.			
Priority u	nder 35 U.S.C. § 119							
	Acknowledgment is made of a claim for foreign	priority unde	r 35 U.S.C. § 119(a)	-(d) or (f).				
'-	☐ All b)☐ Some * c)☐ None of:							
ł	1. Certified copies of the priority documents							
	2. Certified copies of the priority documents		, -					
	3. Copies of the certified copies of the prior	*		d in this National	Stage			
* 0	application from the International Bureau	•	, ,,	لــ				
3	ee the attached detailed Office action for a list	or the certifie	•		<b>^</b>			
			PAUL DINH PRIMARY EXAMIN	IER Paul	Dinl	<u> </u>		
Attachment								
	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948)	4	) Interview Summary ( Paper No(s)/Mail Da					
3) 🔲 Inform	nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) No(s)/Mail Date		Notice of Informal Pa		O-152)			
U.S. Patent and Tro PTOL-326 (Re		tion Summary	Par	t of Paper No./Mail D	ate 20060403	3		

Application/Control Number: 10/709,798

Art Unit: 2825

### **DETAILED ACTION**

This office action is in response to application 10/709,798, filed on 5/28/2004. Claims 1-20 are pending in this application.

## Claim Objections

- 1. Claims 5-6 and 15-16 are objected to because "wherein the step of identifying failing gates" lacks antecedent basis. It appears that the applicant means: --wherein the step of determining any failing gates--.
- 2. Claim 12 is objected to because "wherein the step of compiling includes compiling" lacks antecedent basis. Appropriate correction is required.
- 3. Claims 10 and 20 are objected to because "where in" should be changed to "wherein".

#### Reasons for Allowance

4. Claims 1-20 would be allowable because the prior art does not teach or suggest a method for identifying and preventing logic errors in an integrated circuit caused by gate oxide leakage having combinations of steps and elements in the claims including particularly the following limitations in claim 1 and similarly recited claim 11: determining, for each driving circuit, the weakest pull-up circuit and the weakest pull-down circuit and converting them to equivalent resistances; defining and modeling, for each net, a comprehensive DC resistance network of the driving circuit resistance, the interconnect resistance, and the current source resistance; determining, for each sink transistor gate, the net pulled up and the net pulled down to determine a DC solution of the gate voltage offset at each sink transistor gate; determining any failing gates with a

Application/Control Number: 10/709,798

Art Unit: 2825

reference level voltage check of the gate voltage offset relative to a given threshold; using a static noise analysis tool to combine the determined gate voltage offset as a noise source with other noise sources, and performing a sensitivity analysis to determine the effect of the noise on the function on each receiving circuit gate; and redesigning each failed net.

## **Conclusion**

- 5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Young et al. (6,378,109) teaches: locating and compiling every net (a netlist is created which defines interconnectivity, Col 5, lines 5-10), which is an interconnect between a driving circuit and a receiving circuit, in an integrated circuit; determining, for each receiving circuit, the gate area (see Figure 11) of each current sink transistor device; and determining, for each receiving circuit, the entire current source to current sink resistive interconnect network (see Figure 5). Young does not teach or suggest all the elements recited in the claims.
- 6. Prosecution on the merits is closed in accordance with the practice under *Ex* parte Quayle, 1935 C.D. 11, 453 O.G. 213.

  A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

Application/Control Number: 10/709,798

Art Unit: 2825

And Links 2005

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAUL DINH PRIMARY EXAMINER Examiner AU 2825